AMENDMENTS TO THE SPECIFICATION

Please substitute the following replacement paragraphs for like-numbered paragraphs of the specification:

[0062] Each memory circuit/compare circuit pair (e.g., memory circuit 528_0 and compare circuit 526_0) may be formed as a content addressable memory (CAM) cell. The CAM cell may be any type of CAM cell including ~~be~~ binary (capable of storing and comparing two logic states) or ternary (capable of storing and comparing three states - logic 1, logic 0 and don't care). The SEL signal lines 530, in this example, represent match lines of the CAM cells. In an alternative embodiment, select logic 524 is a programmable decoder.

[0068] During segment 0 (e.g., during a first clock cycle), input signal line 533_0 carries bit 0 of input string 700 as IN0, input signal line 533_1 carries bit 1 of input string 700 as IN1, input signal line 533_2 carries bit 2 of input string 700 as ~~IN1~~IN2, and input signal line 533_3 carries bit 3 of input string 700 as ~~IN1~~IN3. During this segment, SSDATA is equal to a logic zero state to indicate that segment 0 of input string 700 is present on the CBUS. SSDATA is compared with the stored states in memory circuits 528 and each of SEL_1 and SEL_0 are set to high logic states indicating matches with data stored in memory circuits 528_1 and 528_0, respectively, while SEL_3 and SEL_2 are set to logic zero states indicating mismatches with data stored in memory circuits 528_3 and 528_2, respectively. Since SEL_1 and SEL_0 are in logic one states and memory storage elements $602_{1,1}$ and $602_{0,0}$ are programmed with logic one states, the input bits 1 and 0 of segment 0 of input string 700 are coupled to Y_1 and Y_0, respectively, and are loaded into bits 1 and 0 of the comparand register. Since SEL_3 and SEL_2 are set to logic zero states, IN0 and IN3 are not transferred to Y2 and Y3, respectively, because transistors 606 are off, and the corresponding locations in the comparand register are not updated. In this manner, bits 1 and 0 of input string 700 are filtered from the input string and loaded into bit positions 1 and 0 of the comparand register.

[0073] In this example, SSDATA includes two bits such that up to four segments may be represented. The SSDATA signals may be generated, for example, by processor 310 of Figure 3 or provided by instruction decoder 510 of Figure 5 in response to a compare instruction for input data that is provided over multiple cycles. For example, if the compare instruction indicates that the input string has four segments, the SSDATA bits $SSDATA_1$ and $SSDATA_0$ may be logic

states 00 to represent when the first segment of data is present on the CBUS, 01 to represent when the second segment of data is present on the CBUS, 10 to represent when the third segment of data is present on the CBUS, and 11 to represent when the fourth segment of data is present on the CBUS. For one embodiment, a two-bit counter may be used to cycle through the four states in response to one or more control signals from the instruction decoder. Alternatively, a shift register may be used.